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Ultra-Low Power Transmitter Test Results

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EXECUTIVE SUMMARY

OBJECTIVE

The ultimate objective of the Micro-Power Transmitter (MTX) project is to design, fabricate, and test an ultra-low-power transmitter and integrate it with a non-contact electroencephalogram (EEG)/electrocardiogram (ECG) device to create a prototype that could be sold to a sponsor for further development and manufacture of the device. This report provides the initial test results measured of the fabricated device.

METHOD

SSC Pacific performed testing in the lab using a spectrum analyzer, network analyzer, oscilloscope, computer and a universal serial bus (USB) software protection initiative (SPI) interface to control the device.

CONCLUSION AND RECOMMENDATIONS

The initial test results show that the first design spin of the transmitter has some working components, but overall the design needs to be refined and optimized to perform more reliably and output a higher output power. Test results as well as recommended design changes are provided in the report.

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1. INTRODUCTION

As technology advances and transistor size decreases, electronic devices become more compact and mobile. Whether the application for the electronic device is for data collection, storage, processing, or communication, data passes from one device to another. To make the data transfer easier, wireless data transmission becomes a critical portion of mobile devices. However, a wireless transceiver, especially a transmitter, dominates the power consumption in a mobile device, which limits the operational battery life.

The most widely employed transmitter architectures entail double frequency conversion because it is robust and has proven performance. However, this architecture suffers from high power consumption largely because the system architecture is more complex. Particularly, power amplifiers (PA) and high-frequency phase locked loops (PLL) lead to high power consumption due to high-frequency accuracy and low phase noise requirements.

Recently, several ultra-low power transceiver architectures have been proposed. By employing simple modulation schemes such as amplitude modulation (AM) or on-off keying (OOK), the complexity of the system reduces, thereby decreasing the power consumption [1], [2], [3]. However, these modulation schemes suffer from noise and bandwidth inefficiency [4]. A frequency-based modulation scheme such as frequency modulation (FM) or frequency shift keying (FSK) also has a simple architecture, which consumes low power, but it is still vulnerable to noise and bandwidth inefficiency. A phase-shift keying (PSK) modulation scheme utilizes phase information, therefore it is less susceptible to noise and bandwidth efficient compared to FSK. However, the conventional binary phase shift keying (BPSK) transmitter uses a more complex architecture, and therefore can be more power hungry.

In the previous document [5], we proposed two transmitter designs capable of BPSK modulation that utilizes the injection-locked frequency multiplication (ILFM) technique as reported in [6]. We designed the transmitters with a target power consumption of less than 150 μW and a data rate of 120 kbps. The output frequency targeted was 405 MHz, part of the medical implant communication service (MICS) band. The output power targeted was between -17 and -20 dBm [5]. In this work, the test results of the transmitter designs are reported and analyzed.

2. PRINCIPLE OF ILFM

J. Pandrey and B. P. Otis [6] extensively explained the motivation and the principle of the ILFM. The major goal of the ILFM is to simplify the transmitter architecture and reduce the number of systems operating in high frequency as depicted in Fig. 1. In Figure 1 (a)shows a direct conversion transmitter that consists of a crystal oscillator (XO), a PLL, a mixer, and a PA. In this architecture, systems on the right side of the red dotted line operate in high frequency. In Figure 1(b), a crystal is injection locked to a ring oscillator (RO), and then multiple phase outputs are combined at the last edge combining/ power amplifier (EC/PA) stage. In the latter architecture, only the last EC/PA stage is operating at high frequency. The number of blocks required are reduced and the number of blocks operating at high frequency are minimized. Therefore, the power consumption can be reduced. In [6], FSK modulation is implemented by modulating the oscillation frequency of the XO.

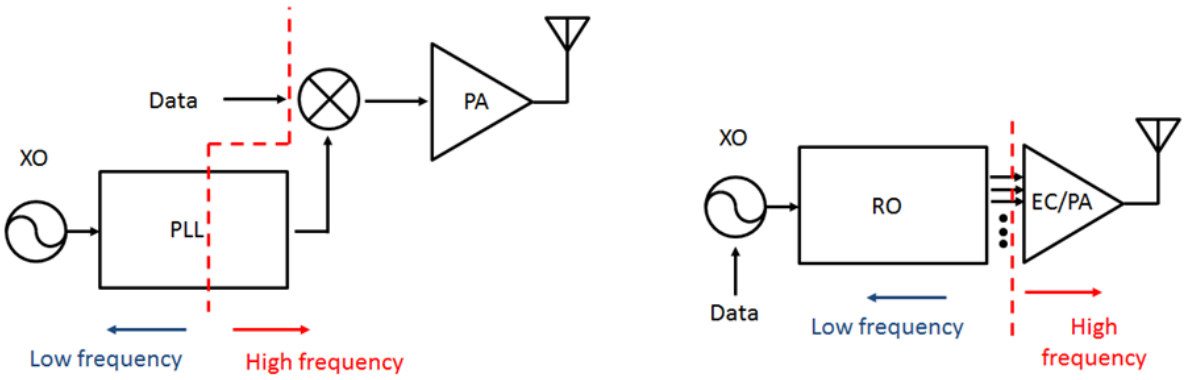


Figure 1. A conventional direct conversion transmitter architecture (a), and an injection-locked frequency multiplication transmitter architecture (b).

In Figure 2, detailed circuit diagrams as well as timing diagrams explain the principle of edge combining. For simplicity, only three stages of the ring oscillator are shown.

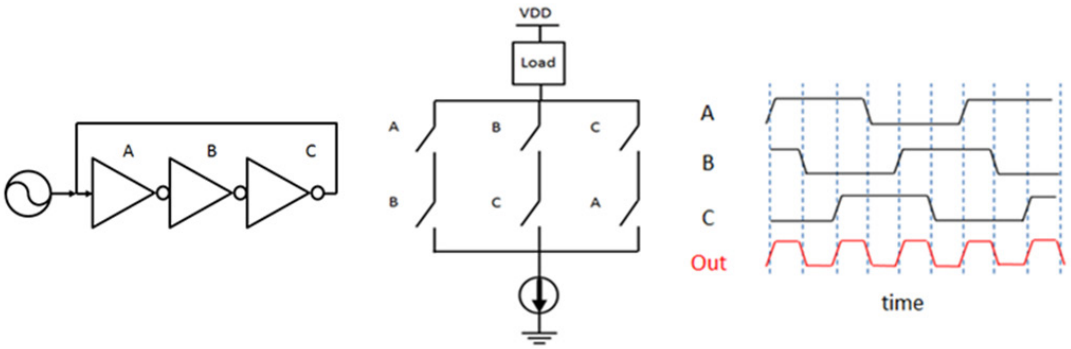


Figure 2. Block diagram of the crystal oscillator injection locking injection locking to the ring oscillator (a), block diagram of the edge combining power amplifier (b), and timing diagram displaying the principle of the edge combining (c).

Using the following architecture, the output can be expressed as

$$\text{Out} = AB+BC+CA \tag{1}$$

Due to the equal delays in the outputs of the RO (A, B, and C) and following the output logic as in (1), the output frequency becomes

$$\text{Fout} = \text{Fxo} \times (\#\text{ of RO stages}). \tag{2}$$

Therefore, increasing the number of RO stages results in a higher output frequency. However, employing a higher number of RO stages also increases the power consumption in the RO stage. In [6], Pandey and Otis used nine RO stages with the XO frequency of 44.5 MHz to generate an output frequency of 400.5 MHz.

Since this circuit is based on digital logic, if a resistive load is used for EC/PA, then the output becomes a square wave. To produce sine wave output, an inductive load can be used to filter out harmonics. An inductive load with a higher quality factor (Q) can suppress the unwanted harmonics better.

3. PROPOSED BPSK TRANSMITTER

Two versions of ultra-low power BPSK transmitter were proposed in [5], as shown in Figure 3.

3.1 TX1: SINGLE ENDED RO

Figure 3 (a) presents the first TX version, which resembles the FSK transmitter as reported in [6]. The architecture is utilizing the fact that when two oscillators are injection locked, frequency and phase are both in sync. Without much change from the circuit proposed in [6], an XOR gate is inserted in between an XO and an RO. Therefore, the power consumption is close to that in [6]. Ideally, the phase of the XO and the RO should be locked, but they may not be, despite the frequencies being synchronized. In addition, there is a transition in phase in the RO stage, which requires extra time for the RO to settle to a new phase.

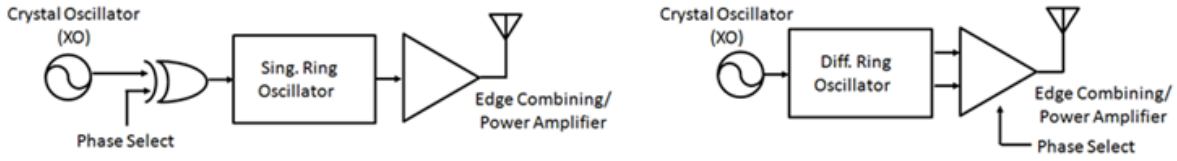


Figure 3. (a) Block diagram of the single-ended TX1, (b) block diagram of the semi-differential TX2, (c) fully differential TX3.

3.2 TX2: DIFFERENTIAL RO

The second TX architecture utilizes a differential RO shown in Fig. 3b. In this TX, the semi-differential EC/PA takes differential phase outputs of the RO, but the output is still single ended, and therefore a single-ended antenna can be used. With the current steering phase select controls, as shown in Figure 5, the output becomes

$$\text{Out} = \text{Phase}(AB+BC+CA)+\text{Phase}'(A'B'+B'C'+C'A'). \quad (3)$$

In this configuration, the RO remains undisturbed and there is a clear distinction between in-phase and out-phase signals. However, the usage of a differential RO requires extra power consumption. Since only one branch of the EC/PA is on while the other branch is off, there is no extra power consumption from the EC/PA compared to the single-ended TX1.

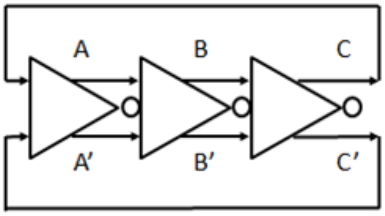


Figure 4. Differential ring.

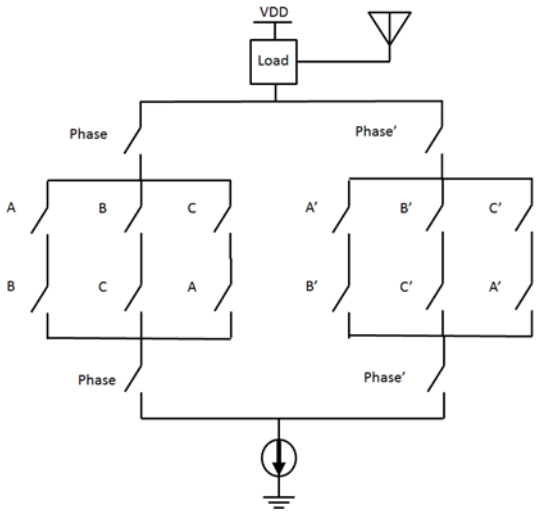


Figure 5. Semi-differential edge combining/power amplifier.

3.3 TX3: DIFFERENTIAL RO AND EC

The third configuration, TX3, shown in Fig. 3c is a fully differential architecture with differential outputs. This configuration also has a fast phase shift function option in which a switch is used to reset after each transition in order for the settling time from bit to bit to be reduced allowing for higher data rates.

3.4 INJECTION LOCKING

Injection locking is a critical operation in this TX architecture to obtain better phase noise without employing a power-hungry frequency generator. The strength of the injection device determines the injection-locking frequency range. A stronger injection device results in a wider locking range. However, if the injection device becomes too strong, it may override the oscillation behavior of the RO. In addition, the stronger injection device means additional uneven loading at the injection point, disturbing the phase at the injection node and creating a reference spur. As a rule of thumb, we recommend that half the strength of the each stage of the RO be used for the injection device.

If the XO was injection locking to the RO as shown in Figure 2 (a), the injection port would have an uneven loading due to the injection device. In [6], a two-stage, multi-point injection is proposed to reduce reference spur and obtain better phase noise. However, this topology still suffers from uneven loading at different nodes. Instead of using a two-stage, multi-point injection, we propose a one-stage injection arranged as in Figure 6. In this configuration, each output node has an equal loading, which results in an even output phase. The injection scheme in Figure 6 can be implemented in a differential RO as well.

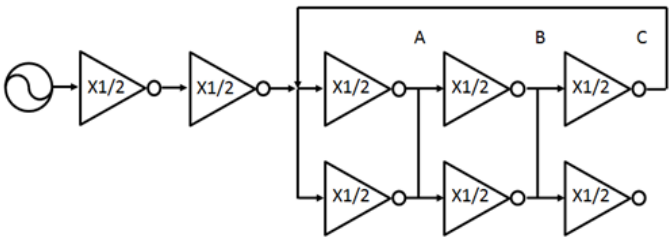


Figure 6. Even-loading, one-stage injection locking in a single-ended representation.

4. TEST RESULTS

Three versions of the transmitter were fabricated and tested. We designed the test boards to easily measure multiple chips while maintaining a majority of the test conditions the same, such as power and voltage/current biasing. Figure 7 shows the test boards, which consist of a motherboard, daughterboard, and chip carrier board.

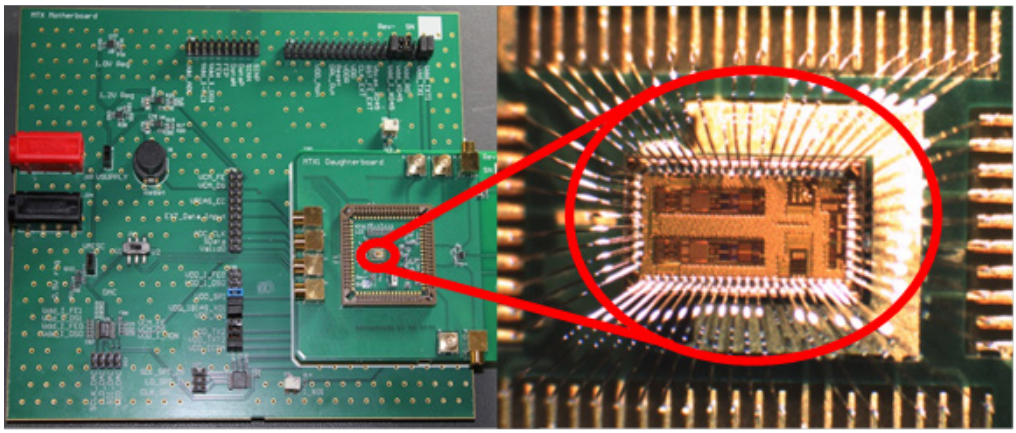


Figure 7. Test boards and close-up view of the microchip.

We measured the crystal oscillator reference for the ring oscillator and oscillates at the desired frequency of 44.84 MHz, which is well within the tolerance specification. The crystal oscillator had an output swing much lower than targeted in design, and the output buffer does not have an output. The only way we could measure the crystal oscillator was to use a high-impedance RF probe on the spectrum analyzer because it has a very low capacitance and the spectrum analyzer has a much higher dynamic range. The amplitude is only a rough estimate because the accuracy of the probe is unknown (see Table 1).

Table 1. Reference XO measurements; measured amplitude is lower than expected.

Parameters	45-MHz Measurements	
	Expected	Measured
Frequency (MHz)	44.833	44.84
Power consumption (μW)	20	22
XO amplitude (Vpp)	0.8	-0.1

Table 2 shows some of the measurements taken on ring oscillator without injection locking. The target frequency was low with a 1-V power supply, but could hit the correct frequency of 400 MHz when Vdd was increased to 1.1 V. However, the power level remained at -33.6 dB, which is quite a bit lower than the target of -20 dBm. This result is probably occurred because the ring oscillator seems to have many harmonics that remove some of the power from the oscillator. This can happen when ring oscillators do not have equal delays at all stages. We also observed that when we turned on the XO for injection locking, the ring oscillator seems to be loaded down even more, and oscillates at an even lower frequency.

Table 2. Stand-alone ring oscillator + edge combining measurements with no injection locking.

RO1_1	RO + EC Amplifier Version 1			
Vdd (V)	Current (μA)	X9 Frequency (MHz)	RO Frequency (MHz)	Power (dBm)
0.8	84.7	186.5	20.72	-40.6
0.9	134.5	257.5	28.61	-36.0
1.0	186.0	329.2	36.58	-35.5
1.1	240.7	401.70	44.63	-33.6
1.2	299.0	475.0	57.78	-33.5

Table 3 shows some results of the ring oscillator with the crystal oscillator turned on for injection locking. The results show the oscillation frequency to be even lower at around 230-MHz output frequency, which is well below the desired 405-MHz target. The ring oscillator probably performs poorly because of bad yield and low amplitude of the crystal oscillator.

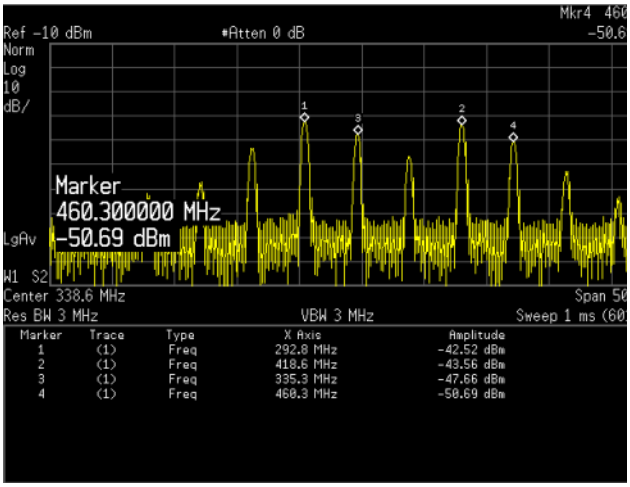
Table 3. Ring oscillator + edge combining measurements with XO injection locking.

RO1	RO + EC Amplifier Version 1			
Vdd (V)	TX Current (μA)	X9 Frequency (MHz)	RO Frequency (MHz)	Power (dBm)
0.9	134.9	230.0	25.56	-36.1
1	187.5	230.0	25.56	-43.0
1.1	248.0	340.8	26.76	-40.6

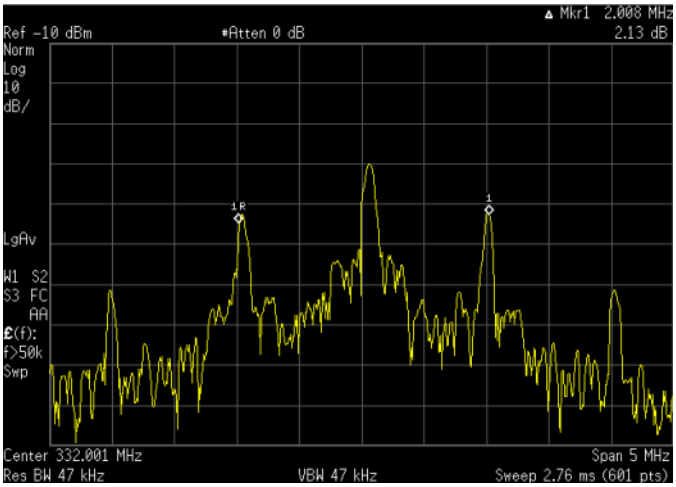
In Figure 8a, the measured output spectrum of TX3 is shown for when the crystal oscillator is off, and when the fast phase shift function is disabled. As shown in Figure 8a, the oscillator has many harmonics that are spaced approximately 42 MHz apart. This means the ring oscillator is not very well balanced and therefore does not have a single primary resonant peak. In Figure 8b, the XO is turned on, which gives the oscillator two major tones and all of the harmonics are reduced by 10 dB or more below the main peaks. This result indicates that the injection locking is working somewhat. Figure 8c shows the spectrum output taken when the transmitter is driven with a waveform of

alternating 1's and 0's at a data rate of 1 MHz. The center peak is the carrier tone and the peaks on each side of the center are the 1-MHz BPSK modulated data. Note that a significant amount of carrier feed-through exists, which is generally bad for BPSK signals. However, when the fast phase transition mode is enabled, the carrier feed-through drops significantly by about 27 dB to about -17 dB relative to the output signals shown in Figure 8d. The fast phase mode has effectively cut down the carrier tone significantly in addition to allowing for higher data rates.

The loop antennas designed for the transmitter were designed as small as possible and therefore do not have much gain at 400 MHz. The designed and fabricated antennas are shown in Figure 9. The return loss plots in Figure 10 show that both antenna designs have a resonant frequency that is very close to the design frequency. The antennas use passive components to tune them to the desired frequency for easy tuning. Figures 10c and 10d show the gain of the antennas is very low because of the small size of the antenna for the operational frequency. The low gain is acceptable since the transmitter design targets short-range communications.



(a)



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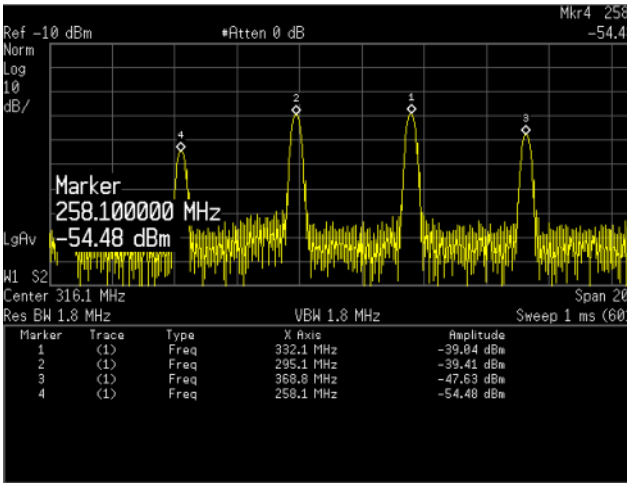

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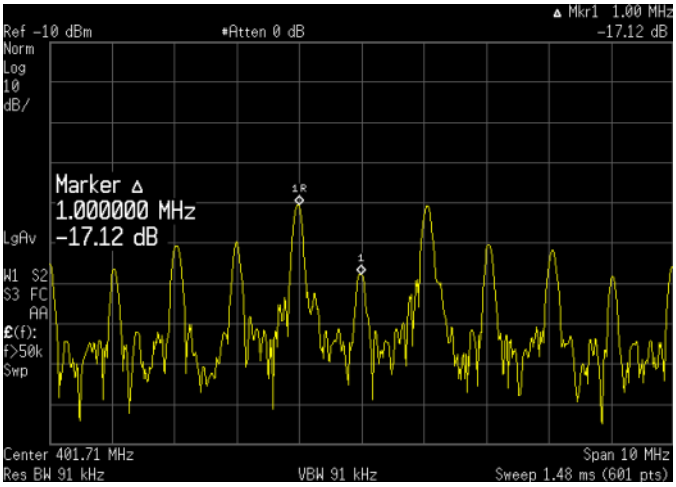


(d)

Figure 8. (a) Output spectrum with no injection locking (a), (b) output spectrum with injection locking, (c) output with 1-MHz input injected into transmitter, and (d) output with fast phase mode enabled.

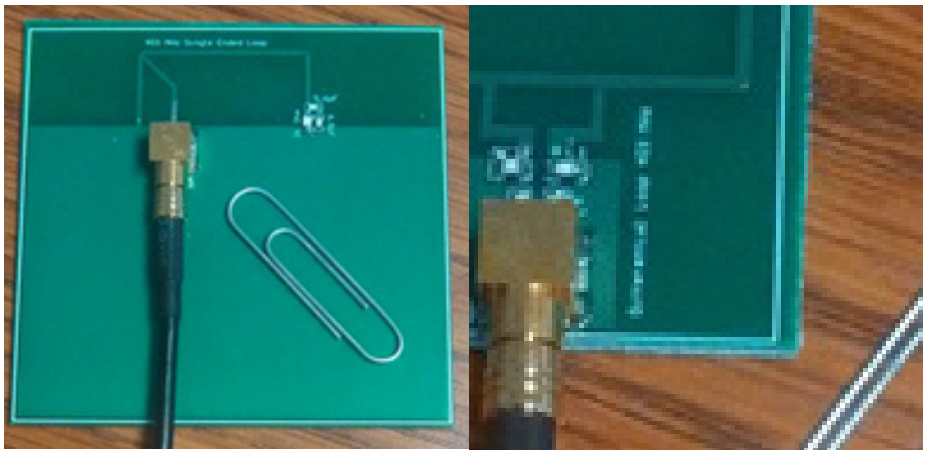
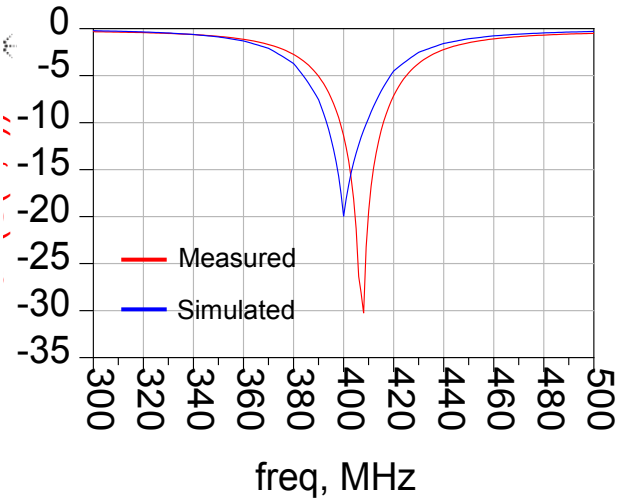
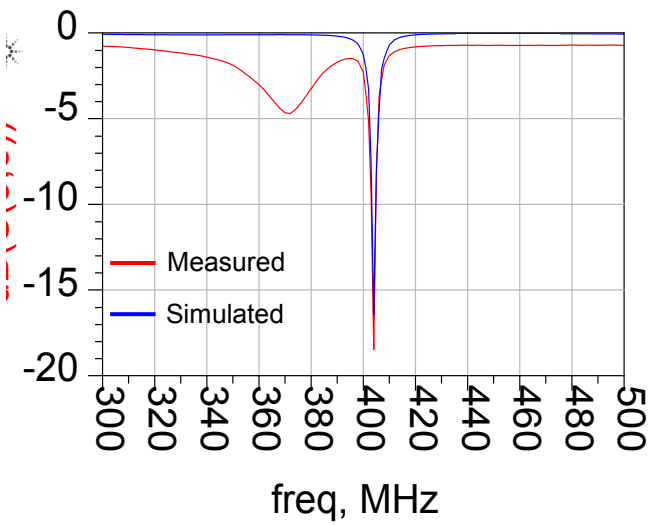


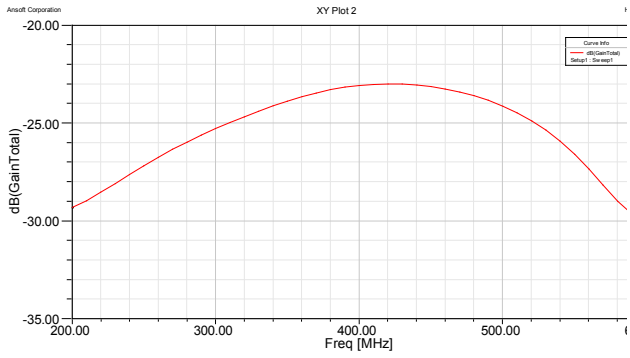
Figure 9. Singled-ended antenna (left) and differential antenna (right).



(a)



(b)



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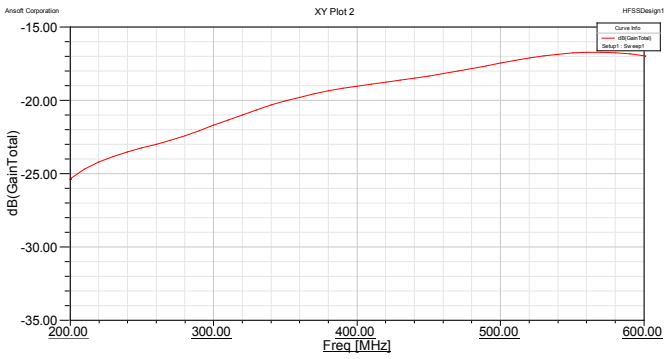


(d)

Figure 10. Plots (a) and (b) show the measured vs. simulated return loss of the single-ended (a) and differential (b) loop antennas. Plots (c) and (d) are the simulated antenna gain plots vs. frequency for the single-ended and differential antenna, respectively.

We tested the ADC design and initial tests show that the ADC is functional. Figure 11 shows the sinusoidal input signal (left) that was used to drive the input and the output spectrum of the ADC (right). The input test signal used was a 24-mVpp sine wave with a frequency of 10 Hz. It was sampled at 330 S/s. The output spectrum shows that the spurious free dynamic range (SFDR) is close to 50 dB.

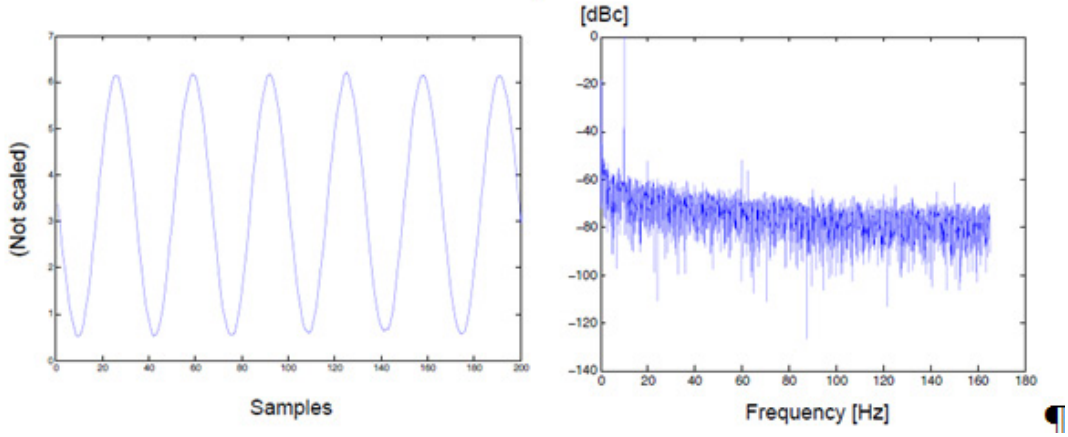


Figure 11. Plots show ADC input signal (left) and output spectrum of ADC (right).

5. TRANSMITTER DESIGN ANALYSIS

Since testing the transmitter, we have re-simulated and analyzed the current transmitter to investigate ways to remove design flaws and improve the design performance. The crystal oscillator had issues with its current mirror because the voltage and current it produced degraded at high temperatures and ±2 sigma. One improvement made to the bias circuit was to remove the NMOS current mirror with an enable switch (see Figure 12) because the extra mirror was not necessary and the switch was stealing current at high temperatures and at ±2 sigma. The PMOS current mirrors used are sufficient to provide the biasing.

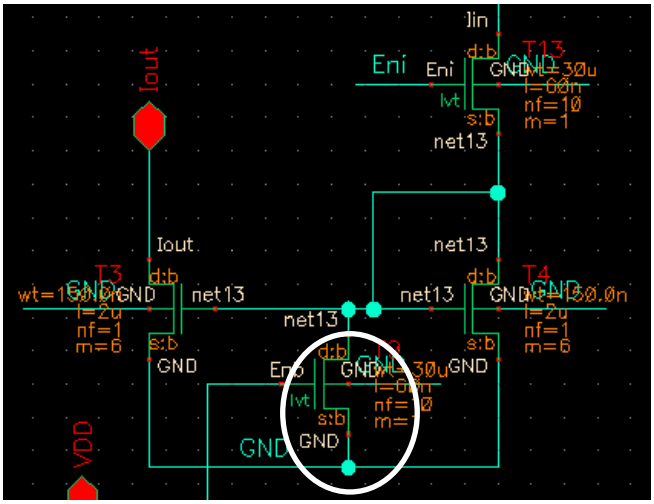
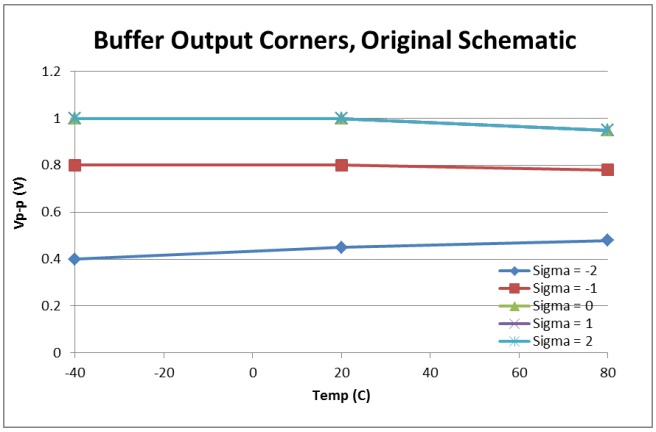


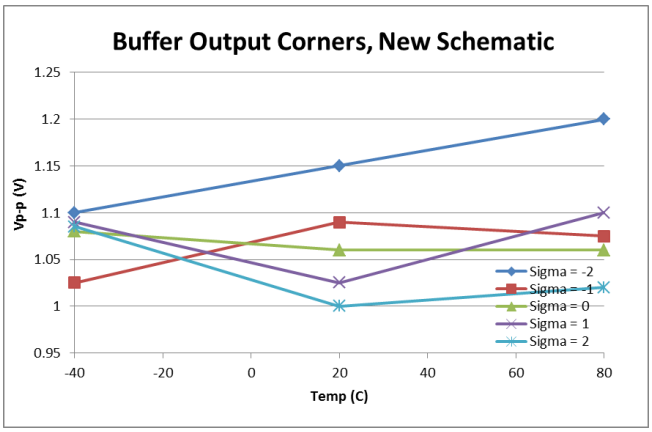
Figure 12. Circled device pulls mirror gate voltage down because of high off-leakage at some corners, which decreases the mirrored current. To solve this problem, the NMOS current mirror was removed because the PMOS current mirror is sufficient to set the current bias.

In addition, the PMOS current mirror device sizes were increased to improve the headroom of the crystal oscillator output. The oscillator output swing was also set to be below 0.6 Vpp so that the oscillation would not push the current mirror out of saturation across all corners. Lastly, the bias voltage, Vbias, was set up using a resistor divider tied to Vdd, with the center point at mid-rail to set the midpoint bias voltage of the output buffer. We also changed the output buffer to have several inverters in series with a PMOS to NMOS width ratio scaled to give the buffer a 50% duty cycle. All of these changes greatly improved the crystal oscillator performance across corners so that the design is much more robust and should provide sufficient output swing no matter the temperature or the process gradient any particular crystal oscillator encounters. See Figure 13 for the results of the simulations both before and after the improvements to the schematic design.

The ring oscillator (or at least the few that were measured) do not seem to oscillate at the correct frequency in the lab when the supply voltage is set to the target of 1 V. A major reason for this is that the ring oscillator design by nature does not have a very tight yield because of its sensitivity to process and temperature variations. Figure 14 shows the histogram of frequencies the original ring oscillator hits over the Monte Carlo simulation of 100 runs. The oscillation yield is spread over a large range of frequencies. However, around 71% of the runs are within ±20 MHz of the target frequency. Figure 15 shows a histogram of output frequencies with injection locking enabled. Around 67% of the runs show that the ring oscillator is locked at the correct frequency by the crystal oscillator. This means the current design should have a yield of around 67%. However, based on the small sample size it is unclear from test results whether this true. However, due to the low swing of the crystal oscillator, this could be the major reason that injection locking is not happening properly, except in a few select cases.



(a)



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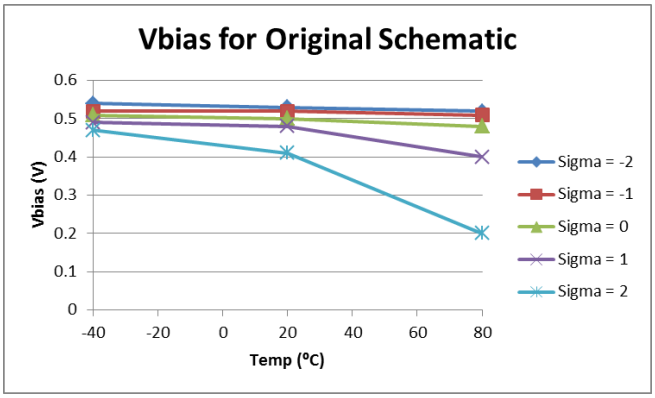
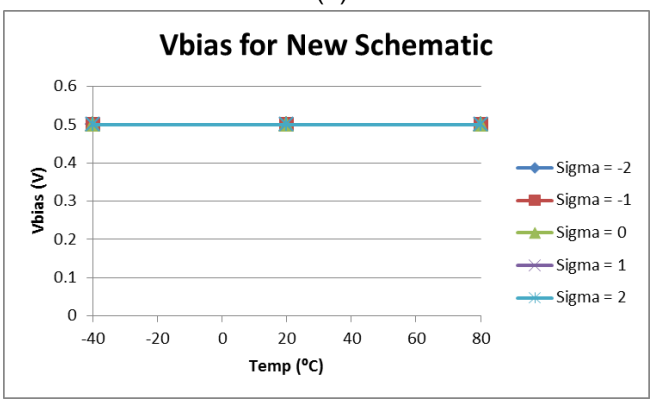


(c)



(d)

Figure 13. (a) and (b): The output of the crystal oscillator has improved greatly with the design fixes as the signal swing is always above 1 V across temperature and process corners. (c) and (d): Vbias was greatly improved across temperature and process corners by switching to a resistor divider to set the voltage mid-rail. Since the resistors track each other across process and temperature, the voltage only moves by hundredths of a volt.

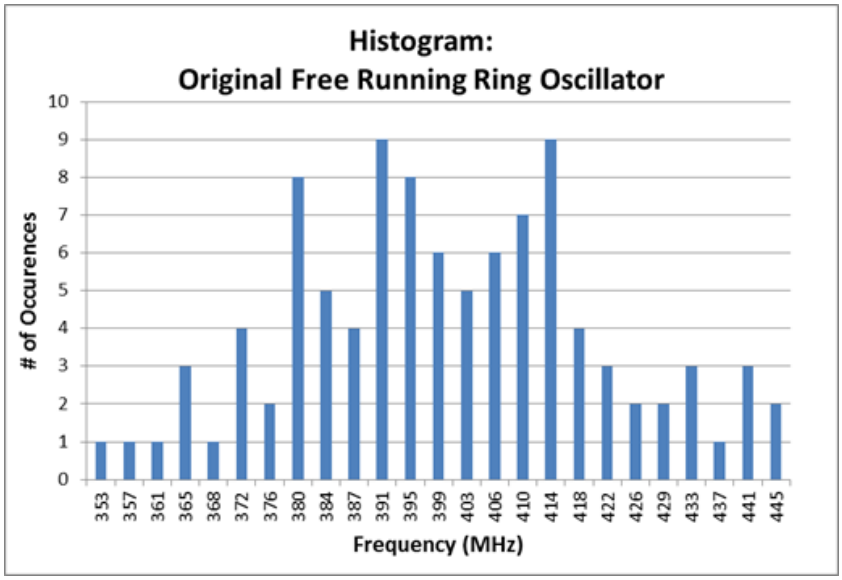


Figure 14. Monte Carlo simulation of free running ring oscillator.

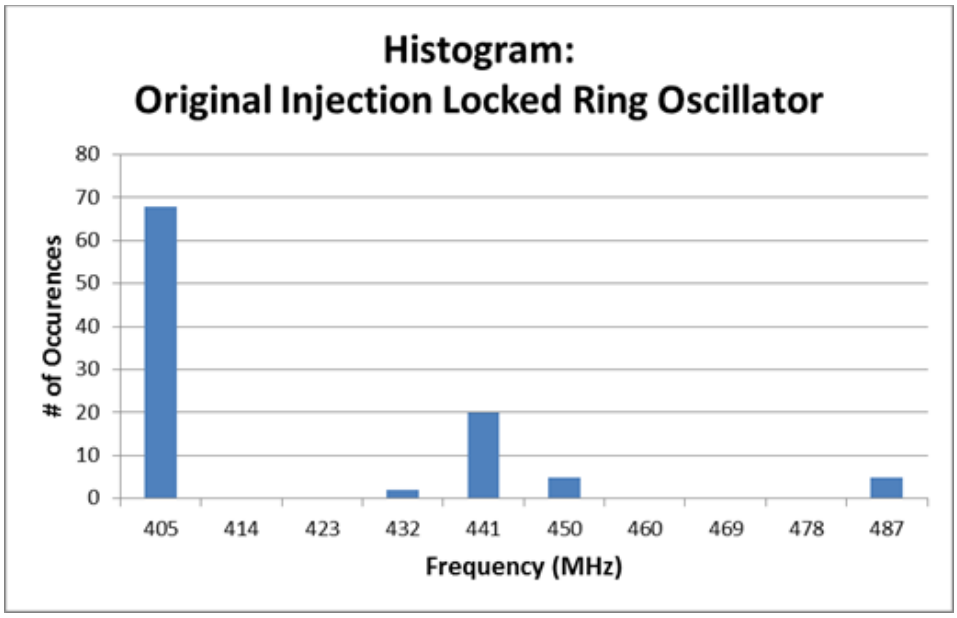


Figure 15: Monte Carlo simulation of injection-locked ring oscillator.

As shown in Figure 16, the yield of the output power for the ring oscillator + edge combing amplifier varies by a wide range as well. A 14-dB spread for all of the runs that locked at the targeted frequency of 405 MHz. We anticipated that with the existing edge combining amplifier, adding 2 bits of coarse tuning to the bias current to allow for four different current settings affects the output power. We can use a similar idea in the ring oscillator to further improve the yield in hitting the target frequency. One way to do this is to add binary-sized inverters that are in parallel to each other with switches in series that can be turned on and off, therefore changing the effective delay of each stage. This design enhancement was explored somewhat. Figure 17 shows the original inverter design used and the new proposed tunable inverter. Using the new design, one could in theory set the inverters to tune the ring oscillator as close as possible to the desired oscillation frequency (45 MHz) and greatly improve the chances that the ring oscillator will lock to the crystal oscillator.

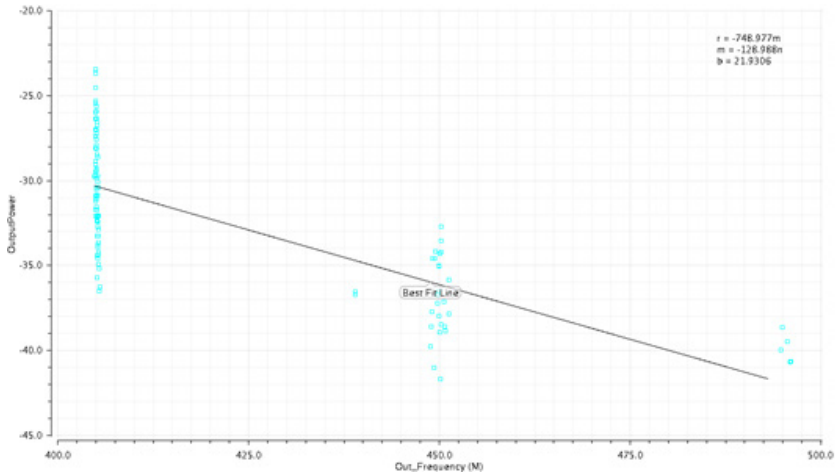


Figure 16. Scatter plot of output power for original ring oscillator design.

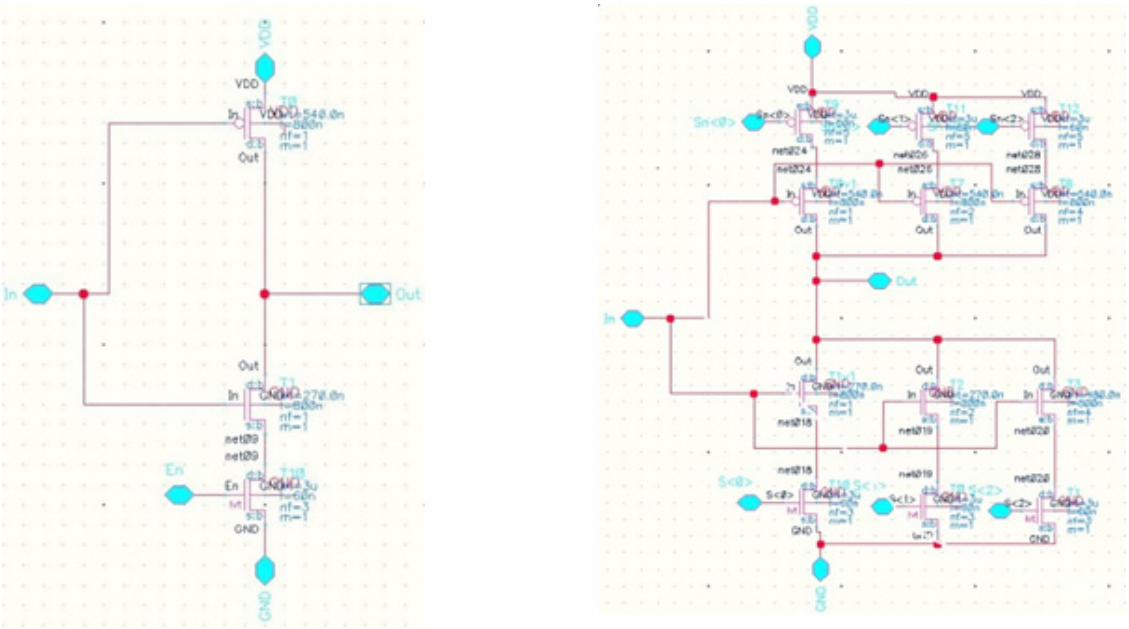


Figure 17. Original inverter (right) and proposed inverter with coarse tuning switches that allow one to enable or disable the parallel inverters (right).

6. CONCLUSION

SSC Pacific explored three architectures of the ultra-low-power transmitter. The architectures were designed, fabricated, and tested. The overall functionality of the chip worked to some degree, but with lower performance than expected. The results varied and the chips were unreliable as measurements made on each chip were inconsistent. Furthermore, the chip design does not seem to be very robust against damage, as some chips stopped working after some amount of testing. The team made design recommendations to improve the chip and make it more robust. The chip will need to be re-designed and fabricated again to fix issues uncovered by testing. If the second revision of the chip is fully functional, then the next steps can be used to integrate the transmitter with an EEG/ECG sensor.

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14. ABSTRACT

There is a growing need in the armed forces for small, low-profile, electronic devices that can easily be concealed and/or worn in clothing. These tiny devices can be worn by warfighters to monitor their health status as well as their location and any other sensor data that is desired. The data can be sent over a wireless link to a mobile device. Conventional transmitter have high power consumption for this application. In this reprot, we test two versions of ultra-low power binary phase-shift keying (BPSK) transmitters, which were designed and fabricated in an IBM 65-nm process. These transmitters employ injection-locking frequency multiplication for near-field (~ 2-m) communication. The power consumption of the proposed transmitters ranges from 90 to 125 μW with the target data rate of 120 kbps.

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Mission Area: Communications

ultra-low power transmitter	injection-locking frequency modulation	binary-sized inverters
binary phase-shift keying	transmitter design analysis	ring oscillator

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